CLOCK GENERATION SYSTEMS AND METHODS

[0001] This application is related to co-pending application Ser. No. _____ entitled "SYSTEMS AND METHODS FOR TESTING WIRELESS DEVICES," filed concurrently herewith and commonly assigned, the content of which is hereby incorporated by reference.

BACKGROUND

[0002] The present invention relates to systems and methods for generating a clock signal.

[0003] To address the ever-increasing need to increase the speed of computers to process ever increasing amounts of data, computer designers have increased the clock frequency of a computers central processing unit and/or utilized parallel processing. Many electrical and computer applications and components have critical timing requirements that require clock waveforms that are precisely synchronized with a reference clock waveform. As discussed in U.S. Pat. No. 6,236,278, to generate a high frequency clock from a lower frequency reference clock, a phase-locked loop ("PLL") is typically used to provide an output signal having a precisely controlled frequency that is synchronous with the frequency of a reference or input signal. In microprocessors, for example, an on-chip PLL can multiply the frequency of a low frequency input (off-chip) clock to generate a high frequency output clock that is precisely synchronized with the lower frequency external clock. Due to the high clock frequency, power consumption for each device has also increased. For certain products such as laptop or notebook computers, handheld computers, cellular telephones, and other wireless personal digital assistants that are designed for situations where power outlets are not available, the conservation of power can be important.

[0004] In a parallel trend, electronic devices that employ short-range radio links have found their way into the daily lives of many people within the past decade. Widespread applications include cordless phones, keyless entry for automobiles, garage door openers, and file transfer in portable computers. Current uses however, are in general restricted to single devices (two transceivers) or a group of very similar devices (e.g., laptop computers). Two recently initiated industry projects, Bluetooth and HomeRF, promise to broaden the use of wireless connections by specifying standard links for a wide range of electronic devices. Bluetooth and 802.11b radios utilize the publicly available 2.4 GHz ISM frequency band for transmission. Operation in this band does not incur usage fees or licenses and permits global use of Bluetooth and/or 802.11b devices.

[0005] Traditionally, multiple integrated circuit chips are required to implement systems offering wireless communications capability. To lower cost, a single chip implementation is needed. However, an integrated circuit with multiple input data ports, the proliferation of multiple phase locked loops and multiple reference clocks may unduly complicate the integrated circuit. Also, a typical digital clock produces a square wave signal in which the harmonics and sub-harmonics occur at the multiples of the clock frequency. With the clock frequency remaining the same, the harmonics are at the same frequency each cycle. These harmonics can interfere with the proper operation of analog components near digital components.

SUMMARY

[0006] In one aspect, a low power reconfigurable processor core includes one or more processing units, each unit having a clock input that controls the performance of the unit; a wireless transceiver transmitting and receiving at a frequency based on a wireless clock input; and a controller having a plurality of clock outputs each coupled to the clock inputs of the processing units and the wireless clock input, the clock outputs being generated from a common master clock.

[0007] Implementations of the above aspect may include one or more of the following. The master clock can operate at up to several Gigahertz, or the master clock can operate at the Bluetooth operating frequency, or the master clock can operate at the frequency specified by the 802.11 standard. The system uses a plurality of clock signals, each independently rate controlled to single destination processing element, in a system on a chip which comprises multiple such processors. In one implementation, these clocks may be all derivatives of a single master clock. In another implementation, the clocks can be gated versions of a master clock, thus retaining a level of synchronous relationship to each other.

[0008] The system can change the clock rate of each processor independently of all the other processors, as a result of a decision or algorithm invoked in order to accomplish some goal, such as power reduction, buffer memory management, or emissions control. The clock rate management may be pre-assigned based upon tasks or routines handled by each processor, or it may be invoked as a result of external or internal system stimuli, including but not limited to user input or thermal management.

[0009] The system allows these changes to occur on-the-fly, during normal operation as the processors' tasks or needs vary. The control of each processor's clock rate may or may not be performed in a centralized manner on the chip. Clock rate control need not be limited to simple clock division, but rather may be more sophisticated and flexible so as to obtain rates such as three-eighths or two-thirds of the driving clock.

[0010] Each processing element may connect to other processing elements through use of buffer memories or FIFOs. A FIFO, for example, may support isosynchronous or even asynchronous read versus write ports, hence supporting mismatched rate processing elements.

[0011] Advantages of the system may include one or more of the following. By clocking the wireless core and processor core using a common reference clock signal, the system simplifies the maintenance of clock signal integrity and minimizes the potential for errors from parasitic reactances, impedance mismatches, crosstalk, dispersion and frequency-dependent skin losses.

[0012] The system also varies the clock signal and the clock period to effectively spread undesirable frequency harmonics spurs over the frequency band because the harmonic frequency created by the clock varies over time. The spurious signal energy at the nominal harmonic frequency is reduced and the energy is spread across the spectrum. As a result, spurious signals and other interferences are reduced.

[0013] The use of a single clock generator for both processor and wireless clock generation also reduces compo-